

# KIOXIA BiCS FLASH™ 3D Flash Memory

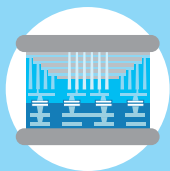
## The Next Generation is Here

The next generation of KIOXIA BiCS FLASH™ 3D flash memory features architectural innovation that meets the needs of data-centric applications like advanced smartphones, PCs, SSDs and data centers. When performance, high density and cost-effectiveness matter, KIOXIA BiCS FLASH™ 3D flash memory delivers.



### Leading the Way

#### Groundbreaking Architectural Innovation



**218 Layers with CBA**  
(CMOS directly Bonded to Array) Architecture



**4 Plane**  
Device




**Lateral Shrink**  
Technology


### Key Features<sup>1</sup>



**80%**  
Interface Speed Increase (3.6Gbps)




**30%**  
Power Efficiency Improvement



**20%**  
Write Performance Improvement



**>10%**  
Read Latency Improvement



**50%**  
Higher Bit Density

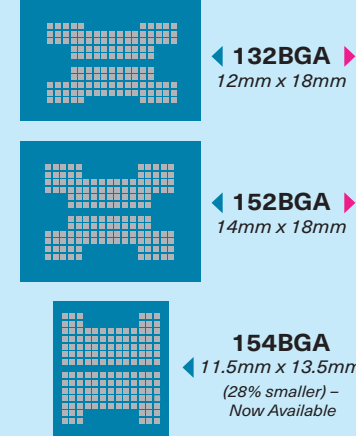


### Densities and Packaging

Industry's First 4TB Single Package Device<sup>2</sup>

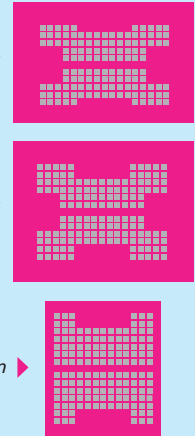
**TLC**  
(Triple-Level Cell)

**1Tb**



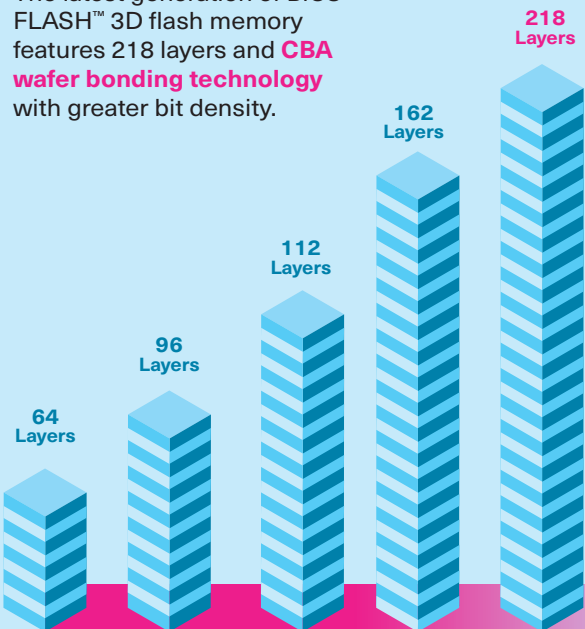
**QLC**  
(Quad-Level Cell)

**1Tb/2Tb**



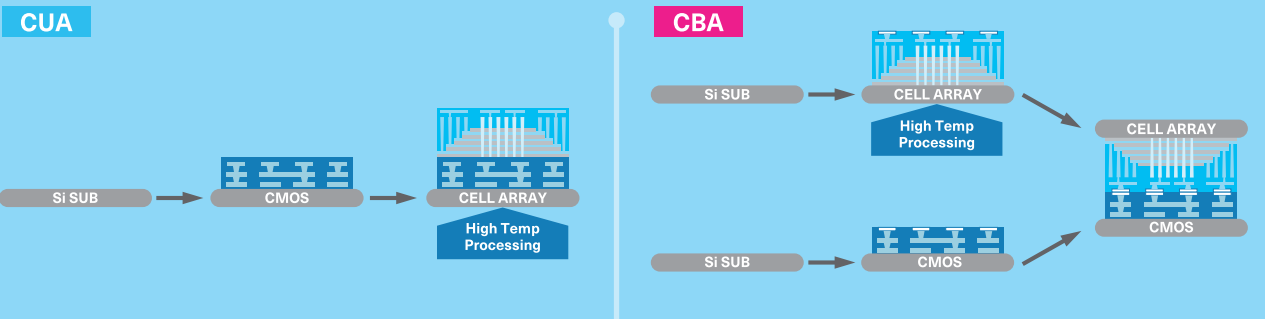
### A Look at Layers

The latest generation of BiCS FLASH™ 3D flash memory features 218 layers and **CBA wafer bonding technology** with greater bit density.



### Why CBA Technology?

KIOXIA has implemented **CBA (CMOS directly Bonded to Array)** technology wherein each CMOS wafer and cell array wafer are manufactured separately in its optimized condition and then bonded together to deliver enhanced bit density and fast NAND I/O speed. Fabrication of the cell and peripheral separately enables optimization of each, eliminating the trade-off between cell reliability and I/O speed.




### Target Applications



IoT



Gaming/  
AR/VR



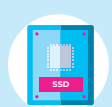
Automotive




Data  
Centers




PCs



Enterprise



Tablets



Smartphones

### Data Center Efficiency

KIOXIA BiCS FLASH™ 3D flash memory was designed to address the most challenging data center issues:

**Density Per Rack Slot**



**Power Efficiency**



**IOPS/QoS**



*The combination of vertical and lateral scaling produces greater capacity with fewer layers – resulting in higher density, smaller die size and optimized cost. Our groundbreaking architectural innovations in lateral scaling and wafer bonding deliver a major leap in performance, density and cost-effectiveness.*

**Scott Nelson**, Executive Vice President & Chief Marketing Officer, KIOXIA America, Inc.